Cheap alternate 4 MB RAM for IIGS

Based to the so called "Garberstreet" RAM card from Briel Computers - this is a description how to make an own 4 MB-RAM card expansion for the Apple IIGS.
In general that RAM-card just is wired for use of 4 pieces of 1 MB SIMM with 30 connection-points and an additional 74 HCT 138 chip for decoding the access to the SIMM modules.

The most difficult challenge will be to get the SIMM-module sockets. Those sockets are available for vertical and laydown plugin. Those use for the angled laydown plugin are preferred because otherwise the card gets rather much "out of balance" when loaded with the SIMM-modules. The best chance to get such sockets will be to pick them of from an old AT PC-board or from one of those common Adaptors out of those days where you could plugin 4 1MB Modules and replace with the adaptor a 4 MB SIMM. When extracting these sockets from the board - take care not to damage the sockets with to much heat.... that will result in bad contact with the modules !

the 1 MB-modules needed for this project have been used most commonly in old 286, 386 and 486 PC systems in the years from 1998 to 2001.

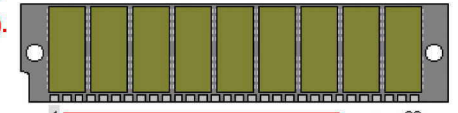
The connector needed for the expansion slot of the IIGS has 44 slot connection contacts - 2 sides with each of 22 contacts.
The cheapest way to get such a connector is to cut it of from an "old-fashioned" 8 Bit ISA-card from the old IBM Computers.....
Those cards have 56 slot-connection-pads so it that connection-part is shortened to 44 connection-pads it will fit.... But be carefull to cut that part within the last pads and remove the goldcovering and adjusting the fit with a fine file and testing the fit to make sure that the contacts are adjusted / centered to the clamps of the socket. Make sure that at least 5 to 7 millimeters of a border are left on top to get a clean and strong glue-area between the socket-connector and the experimental-PCB.

The last page of the description shows how to make a basic fitting board for the mounting and soldering.....
The pages 2 to 6 show in single steps how to make the connections with the wiring. Use thin isolated / covered wire for the task of soldering the connections and follow the steps as shown in the description. For better control please don´t mix up tasks / steps ..... it raises the risk of making mistakes !

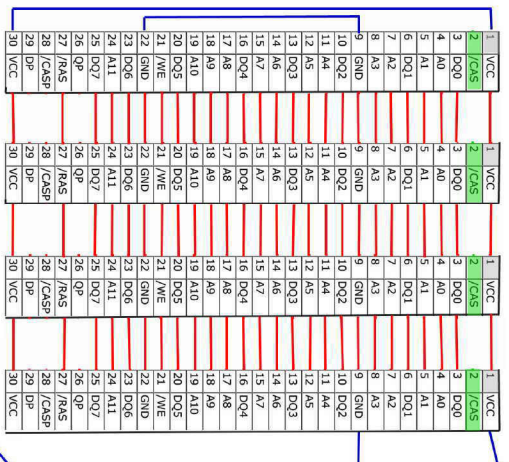
And at the end of the tasks / steps - enjoy the additional RAM in your IIGS !

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8
18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	A11	Address 11
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	/CAS line for the parity RAM on the card *
29	DP	Data Parity In
30	VCC	+5 VDC

First step is to connect the SIMM-modules to rows (common rails).



The second step is to connect the power-source-lines to the module-carriers and the socket as well as to the slot-connector-pads.



74HC/HCT138

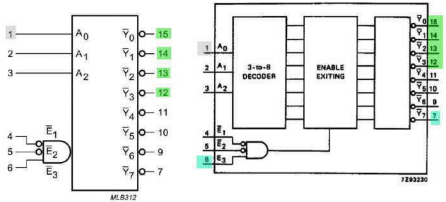
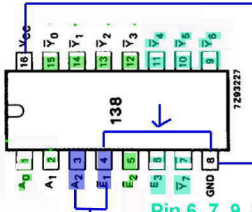


Fig.2 Logic symbol.

Fig.4 Functional diagram.



Pin 6, 7, 9, 10 and 11 are without use and they are not connected !

Pin 3 and 4 must be connected to ground (0 Volt) i.e. "low" -level

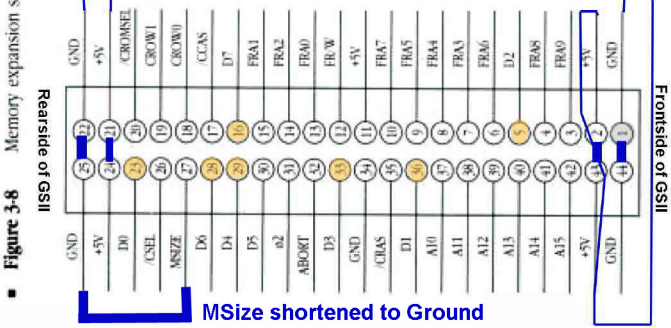


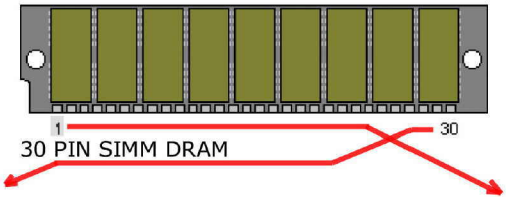
Figure 3-8

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8
18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	A11	Address 11
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	/CAS line for the parity RAM on the card *
29	DP	Data Parity In
30	VCC	+5 VDC

Third step is connecting the adressing-logic of the 74 HCT 138 chip that decodes the use of the SIMM-modules !



SIMM 1

SIMM 2

SIMM 3

SIMM 4

74HC/HCT138

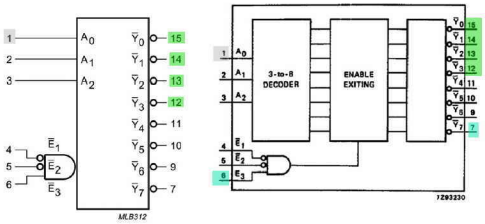
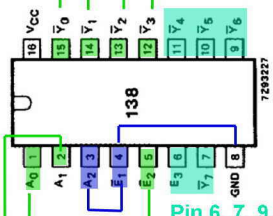


Fig.2 Logic symbol.

Fig.4 Functional diagram.



Pin 6, 7, 9, 10 and 11 are without use and they are not connected !

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

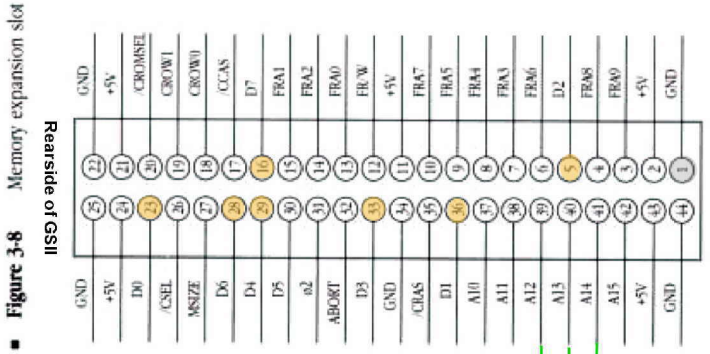


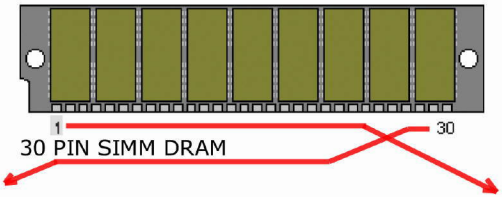
Figure 3-8 Memory expansion slot

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8
18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	A11	Address 11
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	/CAS line for the parity RAM on the card *
29	DP	Data Parity In
30	VCC	+5 VDC

Checkout unused connections !

Checkout that up till now this connections have been made !

Next step will be connecting the datalines DQ0 (SIMM)with D0 (Memoryslot) and so on !



SIMM 1 SIMM 2 SIMM 3 SIMM 4

74HC/HCT138

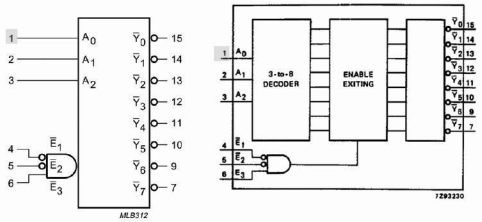


Fig.2 Logic symbol.

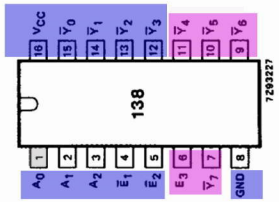


Fig.4 Functional diagram.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

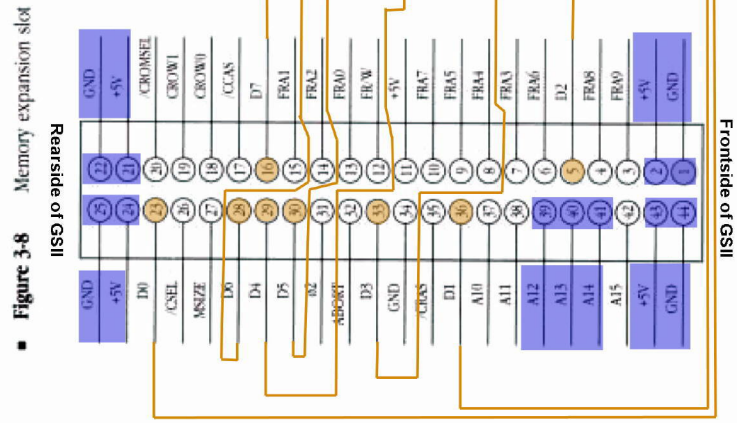


Figure 3-8 Memory expansion slot

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8
18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	A11	Address 11
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	/CAS line for the parity RAM on the card *
29	DP	Data Parity In
30	VCC	+5 VDC

In fact the parity-Bit of the SIMM-modules are not used and therefor may be left without connection !

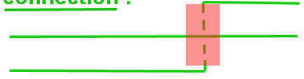
Finished connections.

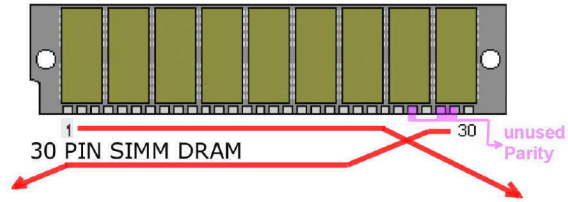
The next step will be to connect the adressinglines from the SIMM-modules (A0 to A9) with the lines of the slotconnector (FRA0 to FRA9) !

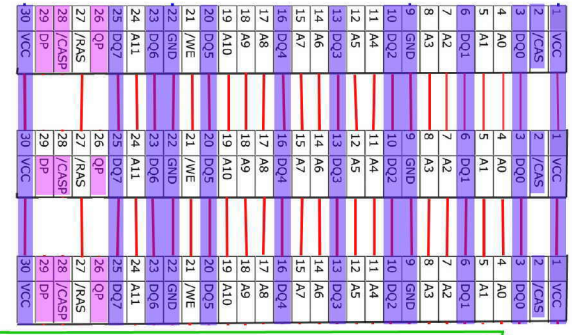
A10 and A11 are not used !

ATTENTION !

Crossing lines WITHOUT connection :







74HC/HCT138

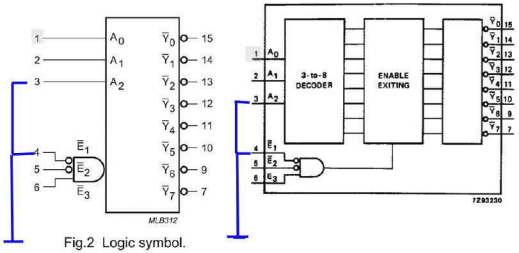


Fig.2 Logic symbol.

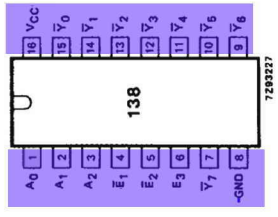


Fig.4 Functional diagram.

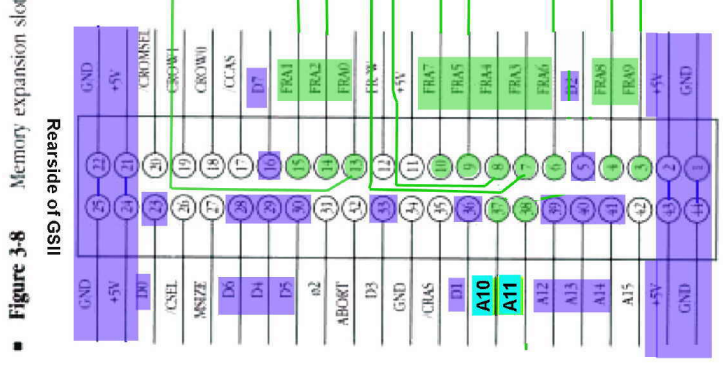


Figure 3-8 Memory expansion slot

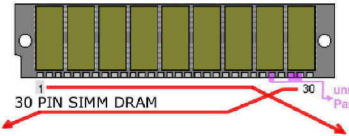
PIN DESCRIPTION

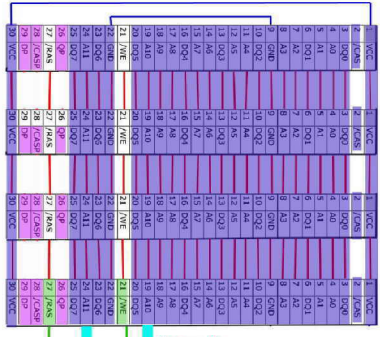
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8
18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	A11	Address 11
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	/CAS line for the parity RAM on the card *
29	DP	Data Parity In
30	VCC	+5 VDC

In fact the parity-Bit of the SIMM-modules are not used and therefor may be left without connection !

Finished connections up till now !





74HC/HCT138

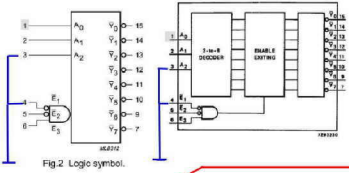
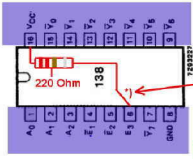


Fig.2 Logic symbol.

Fig.4 Functional diagram.



Important Remark: Allthough the original PCB leaves the pin 6 without connection, in cases that the card does not operate correct - it might be needed to tie the pin 6 with a 220 Ohm resistor up to "high"-level (i.e. to the 5 Volt powerline). In the case that instead of the HCT-version only a LS-version is used - the resistor is obligatory !

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

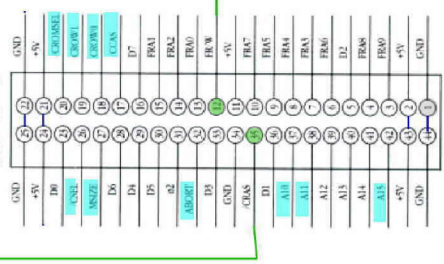
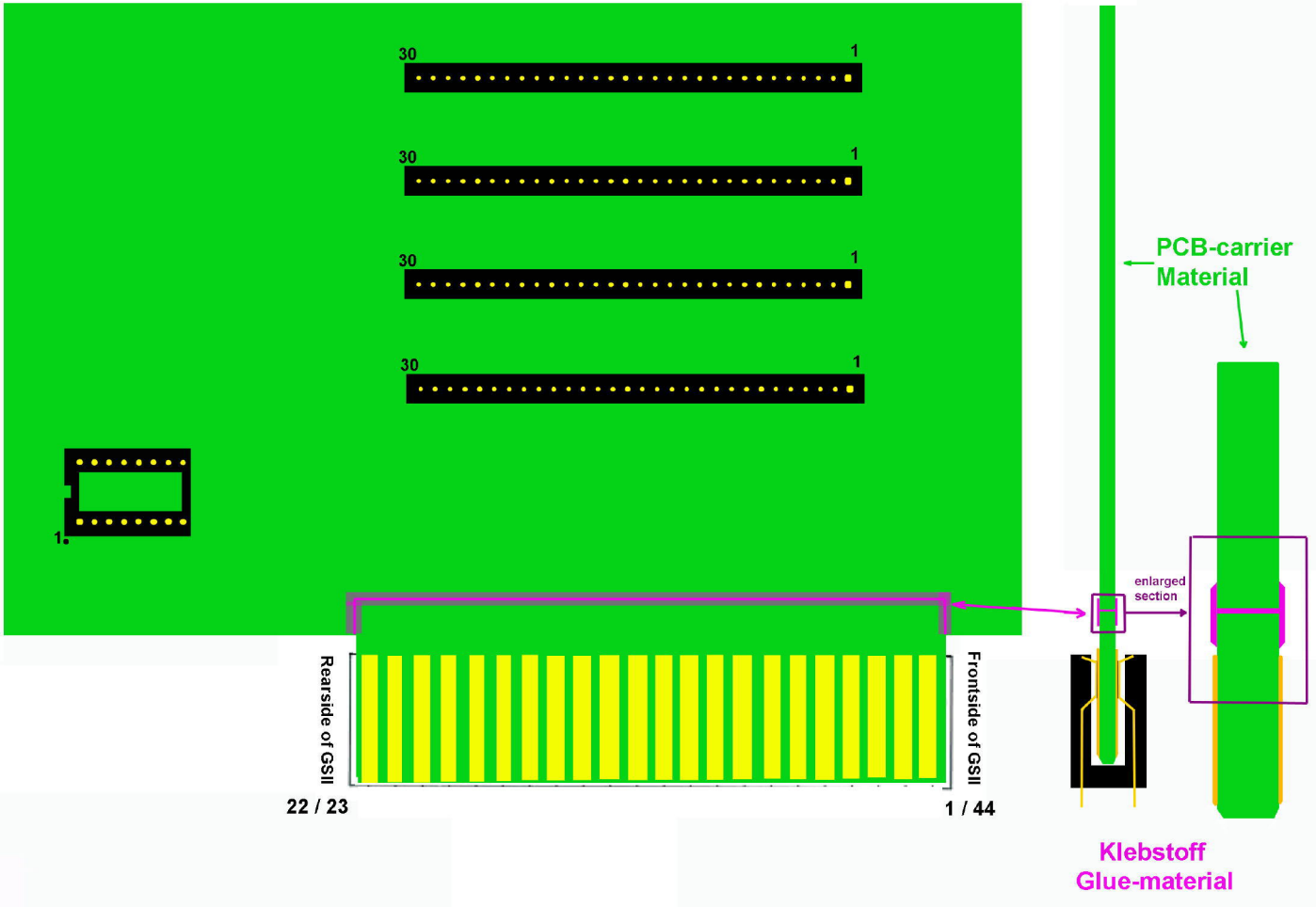


Figure 3-8


30
1
30
1
30
1
30
1
1
PCB-carrier
Material
enlarged
section
Rearside of GSII
Frontside of GSII
22 / 23
1 / 44
Klebstoff
Glue-material